

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of the Claims:

1 Claim 1 (currently amended): A method of performing
2 additive synthesis of digital audio signals in a recursive
3 digital oscillator, comprising:
4 receiving digital audio signal frames wherein each
5 digital audio signal frame includes a set of frequency,
6 amplitude, and phase components represented as coefficients
7 of variables in a mathematical expression, each digital
8 audio signal frame thereby including a frequency coefficient
9 representation;
10 forming converted frequency coefficients by Re-Mapping
11 ~~linearaly re-mapping~~ of bits of said frequency coefficient
12 representation to bias audio reproduction accuracy toward
13 low frequency signals; and
14 performing additive synthesis with said converted
15 frequency coefficients.

1 Claim 2 (original): The method of claim 1 further
2 comprising the step of defining said frequency coefficient
3 representation with an exponent characterizing a
4 floating-point range extension.

1 Claim 3 (currently amended): The method of claim 2 wherein
2 said defining step includes the step of specifying said
3 exponent to correspond to a right shift amount necessary to

4 correct for precision limitations introduced by limiting
5 Re-Mapping ~~re-mapping~~ coefficients to 16 bits.

1 Claim 4 (original): The method of claim 3 wherein said
2 receiving, forming, and performing steps are implemented
3 utilizing a 16-bit fixed point processor.

1 Claim 5 (original): The method of claim 1 wherein said
2 receiving, forming and performing steps are implemented
3 utilizing a digital signal processor.

1 Claim 6 (original): The method of claim 1 wherein said
2 receiving, forming, and performing steps are implemented
3 utilizing a field programmable gate array.

1 Claim 7 (original): The method of claim 1 wherein said
2 receiving, forming, and performing steps are implemented
3 utilizing a Very Long Instruction Word processor.

1 Claim 8 (original): The method of claim 1 wherein said
2 receiving, forming, and performing steps are implemented
3 utilizing a Reduced Instruction Set Computer.

1 Claim 9 (original): The method of claim 1 wherein said
2 receiving, forming, and performing steps are implemented
3 utilizing a Residue Number System processor.

1 Claim 10 (currently amended): A computer readable memory to
2 direct a processor to function in a specified manner,
3 comprising:

4 a first set of executable instructions to receive
5 digital audio signal frames wherein each digital audio
6 signal frame has a set of specified frequency values
7 expressed as a bit sequence;

8 a second set of executable instructions to Re-Map
9 transform said bit sequence to represent lower frequencies
10 with more significant bits and higher frequencies with less
11 significant bits; and

12 a third set of executable instructions to facilitate
13 additive synthesis of said digital audio signal frames in a
14 reduced-precision recursive digital oscillator.

a 1 Claim 11 (original): The computer readable memory of
2 claim 10 wherein said first set of executable instructions
3 include instructions to identify a frequency coefficient
4 representation of said specified frequency.

1 Claim 12 (original): The computer readable memory of
2 claim 11 further comprising a fourth set of executable
3 instructions to define said frequency coefficient
4 representation with an exponent characterizing a
5 floating-point range extension.

1 Claim 13 (currently amended): The computer readable memory
2 of claim 12 wherein said fourth set of executable
3 instructions include instructions to specify said exponent
4 to correspond to a right shift amount necessary to correct
5 for precision limitations introduced by a reduced ~~reduce~~
6 precision processor.

1 Claim 14 (new): A method of performing additive synthesis
2 of digital audio signals comprising:

3 a) receiving a sequence of digital audio signal frames
4 wherein each digital audio signal frame of said sequence
5 includes a set of frequency, amplitude, and phase
6 components; and,

7 b) linearly scaling said amplitude component within
8 each of said frames, frame N, wherein N labels a frame of
9 said sequence, from zero to a peak value for a first portion
10 of said frame N, and from said peak value to zero for a
11 second portion of said frame N, creating thereby a scaled
12 frame partial for frame N; and,

13 c) summing successive scaled frame partials in a
14 overlapping pairwise manner to produce a sequence of summed
15 partials [N, (N+1)], [(N+1), (N+2)], [(N+2), (N+3)]
16 continuing through at least a portion of said sequence,
17 thereby approximating a varying-frequency varying-amplitude
18 frame partial with a sum of two fixed-frequency
19 fixed-amplitude scaled frame partials.

1 Claim 15 (new): A method as in claim 14 wherein said
2 overlapping pairwise summation comprises approximately 50%
3 overlap between members of each pair of said summed
4 partials.

1 Claim 16 (new): A recursive digital oscillator generating
2 frequency f lying in the range from zero to one-half of a
3 sampling frequency f_s comprising:

4 recursion coefficients x_n given by

5 $x_n = x_{n-1} - \epsilon x_{n-1} - x_{n-2}$

6 wherein $\epsilon = 2 - 2 \cos(\omega)$ and

7 wherein $\omega = 2\pi f/f_s$.

A 1 Claim 17 (new): An oscillator as in claim 16 wherein ϵ is
2 represented by an unsigned mantissa, m , combined with an
3 unsigned exponent, e , biased so that the actual
4 represented value is

5 $\epsilon = 2^{2-e} m$.

1 Claim 18 (new): An oscillator as in claim 17 wherein said
2 mantissa m is 16 bits.